Sub-50 nm isolated line and trench width artifacts for CD metrology

M. Tortonese[a], G. Lorusso[b], R. Blanquies[a], J. Prochazka[a], L. Grella[b]
[a]VLSI Standards, Inc., 3087 North First Street, San Jose, CA 95134
[b]KLA-Tencor Corporation, 160 Rio Robles, San Jose, CA 95134

ABSTRACT

We present a technique to produce isolated lines and trenches with arbitrary widths in the range of 12 nm to 500 nm, arbitrary heights and depths in the range of 100 nm to 2 µm, 90-degree sidewall angle, and top corner radii as small as 5 nm. These structures are ideal candidates as Critical Dimension (CD) absolute standards. The sidewall angle can further be varied to create an arbitrary sidewall angle that can be accurately measured.

Keywords: Critical Dimension, CD-SEM, CD-AFM, line edge roughness, line width roughness, LER, LWR

1. INTRODUCTION

Accurate metrology of the width of lines and trenches requires standards for line width and trench width that are traceable to the international system of units (SI). The need for dimensional accuracy grows more critical as the size of structures manufactured shrinks and becomes comparable to the systematic bias of metrology tools such as CD-SEM and CD-AFM. The bias may, in turn, depend on the dimension of the features being measured, which requires a set of dimensional standards of size close to the size of the features being measured to characterize the measurement linearity. The need for traceable dimensional standards in the semiconductor industry has been addressed by researchers at NIST, who have fabricated single crystal silicon structures with vertical and smooth sidewalls in <110> silicon using conventional photolithography and anisotropic silicon etching in an alkaline solution[1].

2. FABRICATION

Our technique consists of depositing a film of a thickness and material equal to the width and material of a desired CD artifact on a silicon wafer, then cross-sectioning, polishing, etching, and presenting the resulting sample to the measurement tool so that the original thickness of the film is measured as a lateral CD. This technique has the advantage of creating artifacts with lateral values of CD that have the uniformity attributes of a film deposition and vertical sidewalls. The value of the CD can be controlled with the same amount of control available in thin film deposition tools, and is scaleable to very small values of CD. This technique is capable of producing trenches with minimal Line Edge Roughness (LER) and Line Width Roughness (LWR).

2.1 Trenches

We have fabricated isolated trenches by growing a thermal oxide on two silicon wafers and bonding them together (Fig. 1a). The bonded pair is subsequently diced into small dies, and each individual die is then thinned and polished on edge (Fig. 1b). Finally the oxide layer is etched back to a desired depth in a buffered oxide etch solution. The depth of the trench is controlled by the etch time. The final sample is 1.45 mm wide x 4 mm long, with the trench running along its entire 4 mm length.

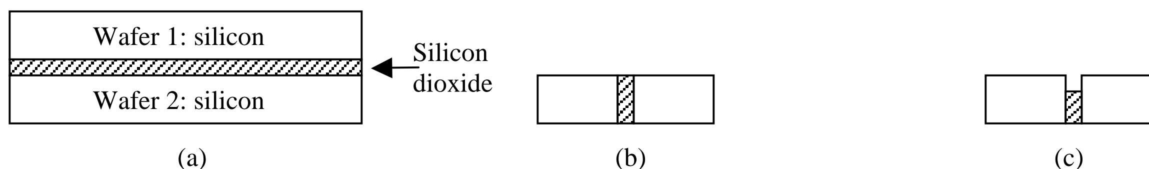

Fig. 1: Method used to fabricate a trench width sample.

Metrology, Inspection, and Process Control for Microlithography XVIII, edited by Richard M. Silver, Proceedings of SPIE Vol. 5375 (SPIE, Bellingham, WA, 2004)
0277-786X/04/$15 · doi: 10.1117/12.536812

Fig. 2a is a view of a nominal 50 nm sample in a CD-SEM. This particular trench was etched to a depth of approximately 2 µm. There is little or no signal originating from the bottom of the trench, which appears dark due to the depth of the etch; therefore, the image contrast is very high. Ideally the LER of this trench would be equal to the surface roughness of the original silicon surface, and the LWR would be equal to the variation in oxide thickness within the field of view. Both these quantities are in the sub-nanometer range. In practice, imperfections in the polishing process can show up as LER and LWR.

Fig. 2b shows a cross-section of a different sample. The cross-section was obtained with a dual beam Focused Ion Beam (FIB)/SEM tool. The sample was first coated with platinum, then cut with the FIB and subsequently imaged at a 52-degree tilt. The silicon was decorated to enhance the material contrast in the image. The image shows the vertical walls of the trench and the surface topography of the sample, with a corner rounding of less than 10 nm as measured from this image.

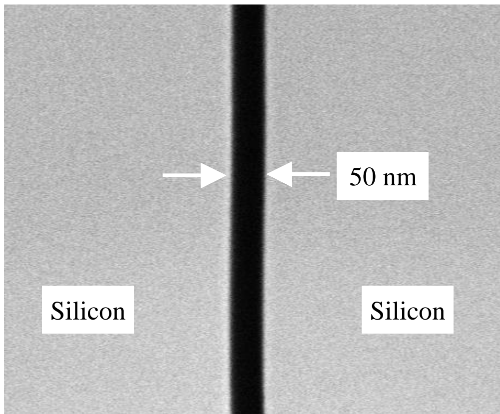

Fig. 2a: CD-SEM image of a trench of 50 nm nominal width, and approximately 2 µm deep.

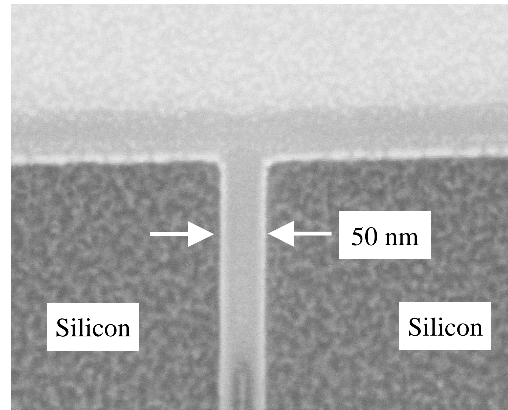

Fig. 2b: Cross-section SEM of a trench of 50 nm nominal width after FIB cut.

Using this technique we have produced trenches with nominal widths of 50 nm, 75 nm, 100 nm, and 500 nm. Figure 3 shows CD-SEM images of these trenches.

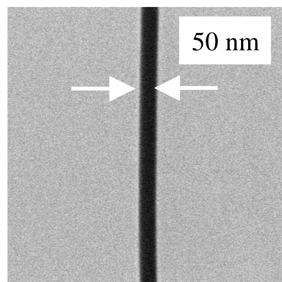

Fig. 3a: 50 nm nominal trench width, 0.75 µm field of view

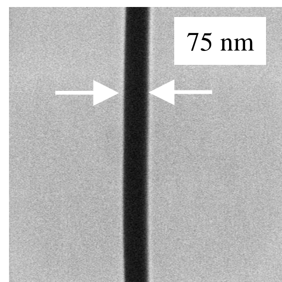

Fig. 3b: 75 nm nominal trench width, 0.75 µm field of view

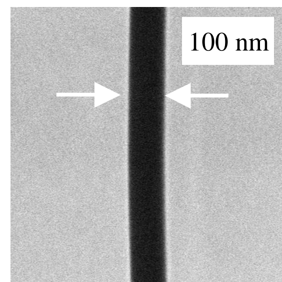

Fig. 3c: 100 nm nominal trench width, 0.75 µm field of view

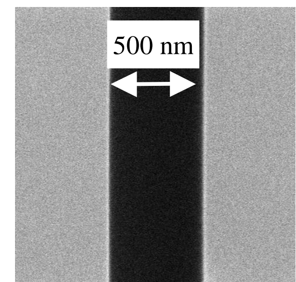

Fig. 3d: 500 nm nominal trench width, 1.5 µm field of view

2.2 Lines

We have fabricated isolated lines using a similar technique as described for the fabrication of trenches, except that instead of a thermal oxide film we have used a more complex film stack. This film stack is composed of a 500 nm thick layer of oxide deposited on top of a silicon wafer, followed by the deposition of a silicon layer of a thickness equal to the desired line width and the deposition of a 500 nm thick layer of oxide and, finally, capped with another layer of silicon. The selection of materials and thicknesses was guided by the objective of producing an isolated silicon line

width that would be perfectly symmetrical with respect to its surroundings. A 50 nm wide line separated from the next silicon structure by 500 nm would correspond to a Line/Space ratio of 10:1. Fig. 4 shows the film stack. For the sake of simplicity, Fig. 4 shows one wafer only, although we have fabricated our samples by joining two such wafers together, like in the case of the trench just described.

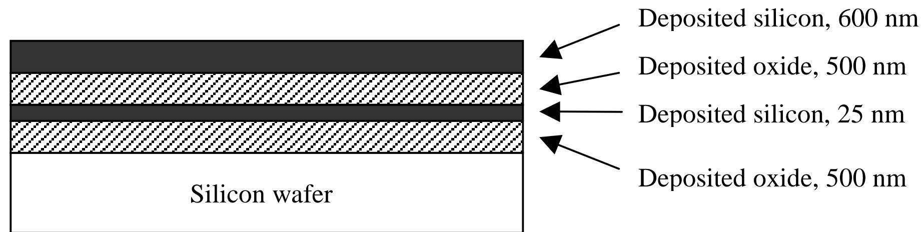

Fig. 4: Film stack used to fabricate a 25 nm line width structure

Following dicing, thinning, and polishing, the sample is etched in a buffered oxide etch solution to produce a line that protrudes out from its surrounding oxide. The height of the line is controlled by the etch time.

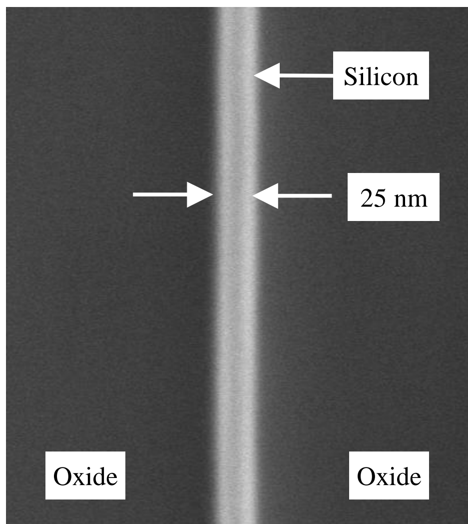

Fig. 5a: CD-SEM image of a line of 25 nm nominal width, approximately 300 nm high. The image shows a length of line of 500 nm.

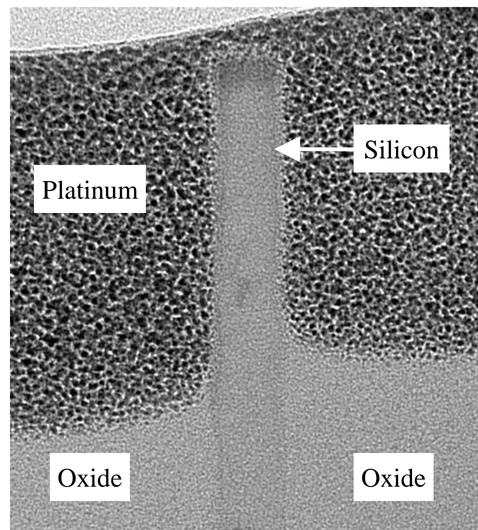

Fig. 5b: TEM cross section of a line of 25 nm nominal width, approximately 100 nm high.

Using this method we have fabricated lines of 12 nm, 25 nm, and 50 nm nominal widths. Figure 5a is a CD-SEM view of a line of 25 nm nominal width and approximately 300 nm high. The height of the line was measured by AFM and confirmed by FIB cross-sections. Figure 5b is a Transmission Electron Microscope (TEM) cross-section of a line of 25 nm nominal width, approximately 100 nm high. For the TEM analysis a small section of the line was coated with platinum and plucked in a dual beam FIB/SEM system. Then it was thinned with an ion mill, deposited on a carbon film, and imaged in a TEM. The top corner rounding can be estimated from the TEM image to be less than 5 nm. The line, as seen in the image, has minimal line width roughness, but some low frequency line edge roughness. The small line width roughness is due to the uniformity of the silicon deposition process, while the line edge roughness is due to the roughness of the thicker oxide layer on which the silicon layer is deposited. As seen in Fig. 5b, the oxide etch is non-uniform and reveals a footing of approximately 25 nm radius. The lack of uniformity is undesirable because it affects the symmetry of the structure. The non-uniformity of the oxide etch is not a problem when the height of the line is 300 nm, because of the high contrast obtained in a CD-SEM from such structures, but it is a problem for shallower structures, where the image contrast is lower.

Using this technique we have fabricated two sets of lines of 12 nm, 25 nm, and 50 nm nominal widths. We etched the first set to produce lines 300 nm high, and the second set to produce lines 100 nm high. The corresponding CD-SEM images are shown in Fig. 6.

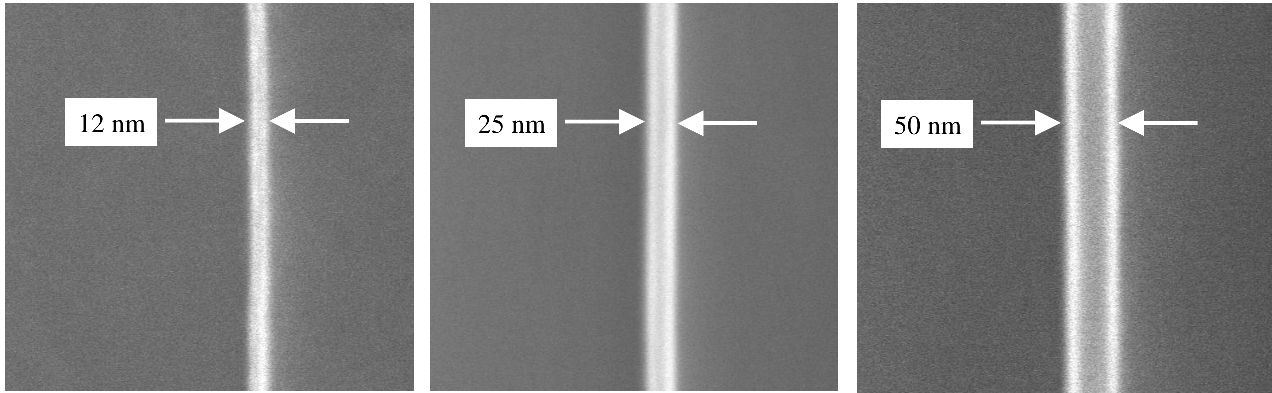

Fig. 6a: Nominal 12 nm wide silicon line, 300 nm high on oxide

Fig. 6b: Nominal 25 nm wide silicon line, 300 nm high on oxide

Fig. 6c: Nominal 50 nm wide silicon line, 300 nm high on oxide

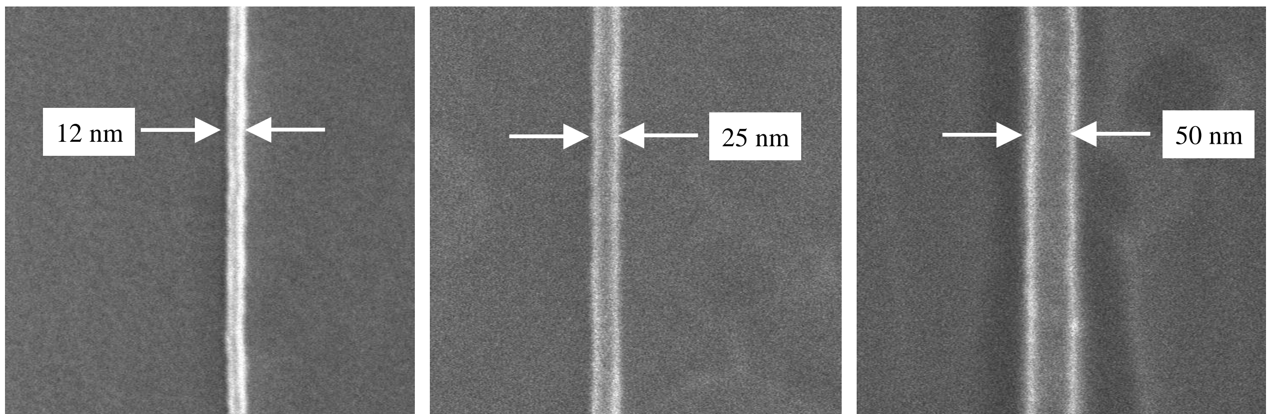

Fig. 6d: Nominal 12 nm wide silicon line, 100 nm high on oxide

Fig. 6e: Nominal 25 nm wide silicon line, 100 nm high on oxide

Fig. 6f: Nominal 50 nm wide silicon line, 100 nm high on oxide

2.3 Mounting into a silicon wafer

The samples resulting from this process are 1.45 mm wide and 4 mm long, with the line running in the middle of the sample, and along its entire 4 mm length. In order to image the samples in a CD-SEM, the samples need to be mounted into a wafer in a way that the surface of the sample is co-planar with the surface of the wafer, and in a way that minimizes any topographic discontinuity between the edges of the sample and the wafer, because large topographic gaps can produce fringing fields around the edges of the chip that can affect the quality of the image. We achieve co-planarity and reduce topographic gaps between the sample and the wafer by first mounting the sample into a silicon die in which a square hole has been microfabricated. This die is then mounted into a pocket etched out of a silicon wafer using a technique described elsewhere[2]. The two mounting steps are referenced to the surface of the die and to the surface of the wafer, respectively, to achieve co-planarity. Fig. 7 shows the samples mounted into a 200 mm wafer using this technique.

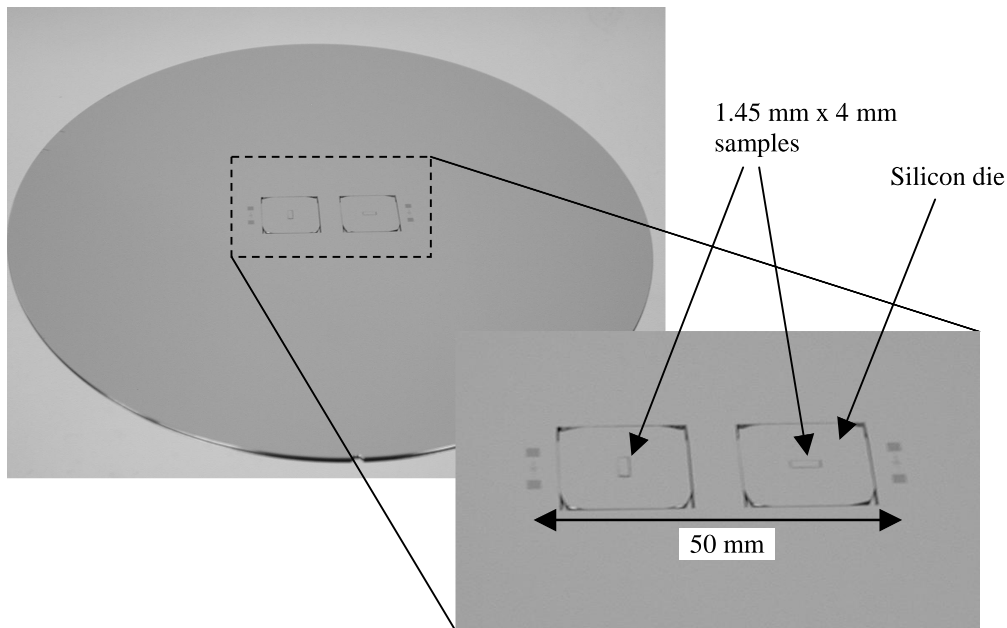

Fig. 7: Two samples mounted into a silicon wafer. The two samples are mounted one horizontally, the other vertically so as to be able to test both scanning directions.

3. TRACEABLE MEASUREMENT OF THE CRITICAL DIMENSION

The samples discussed so far are good candidates to become calibration standards for CD-SEM and CD-AFM because they have the following quality attributes: 1) the CDs that can be produced are comparable to the dimensions of lines that need to be measured in a semiconductor manufacturing process; 2) the uniformity of the line width appears to be much smaller than the line width itself; and 3) the length of the line available is a few millimeters, which enables a reasonable lifetime for the standard, even when used in a hydrocarbon contaminating CD-SEM environment. For these samples to become dimensional standards traceable to the international system of units, they must be measured against a known reference, and an uncertainty must be associated with the measurement, within a specified level of confidence.

We propose to measure these samples from TEM images calibrated against the silicon atomic lattice spacing present in the sample itself. The traceability work is non-trivial, and is not discussed in this paper. Factors to be considered are the presence of a native oxide layer, the uniformity of the line width or trench width, the uncertainty in the determination of the edge of the structure from the TEM image, the screen linearity of the TEM imaging system, the stability of the samples over time while exposed to a variety of environmental conditions, just to mention a few. In addition, the practical conditions of use must be considered, such as the hydrocarbon contamination build up when imaging with a CD-SEM.

In this section we illustrate the concept of how these samples could be made traceable to the international system of units and point out to some of the challenges.

3.1 Trenches

Fig. 8 shows a High Resolution TEM (HRTEM) image of a cross-section of a 50 nm trench. The sample was prepared for the TEM image by mechanical polishing. We have used the silicon lattice structure to the right of the structure to calibrate the magnification of the image. Using this procedure we have measured the trench width to be 48.6 nm. This does not in itself constitute a traceable measurement because it is not accompanied with a statement of uncertainty. Nevertheless, this example shows the traceability path that could be used to obtain a traceable measurement of the trench structure.

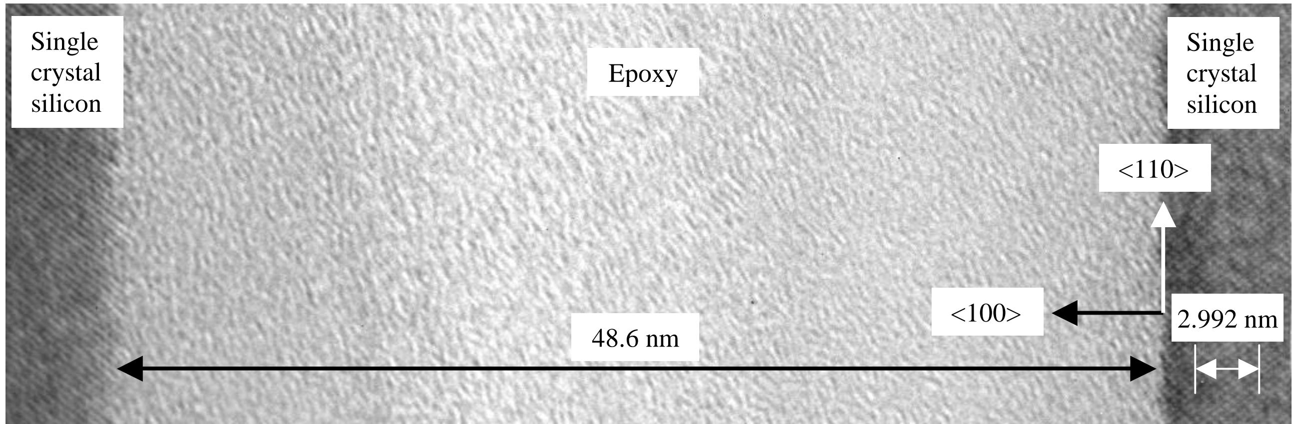

Fig. 8: HRTEM of a trench sample showing the crystallographic planes and the width of the trench measured against the scale provided by the silicon atomic lattice spacing.

3.2 Lines

Fig. 9 shows three TEM images of a cross-section of a 25 nm nominal line width sample.

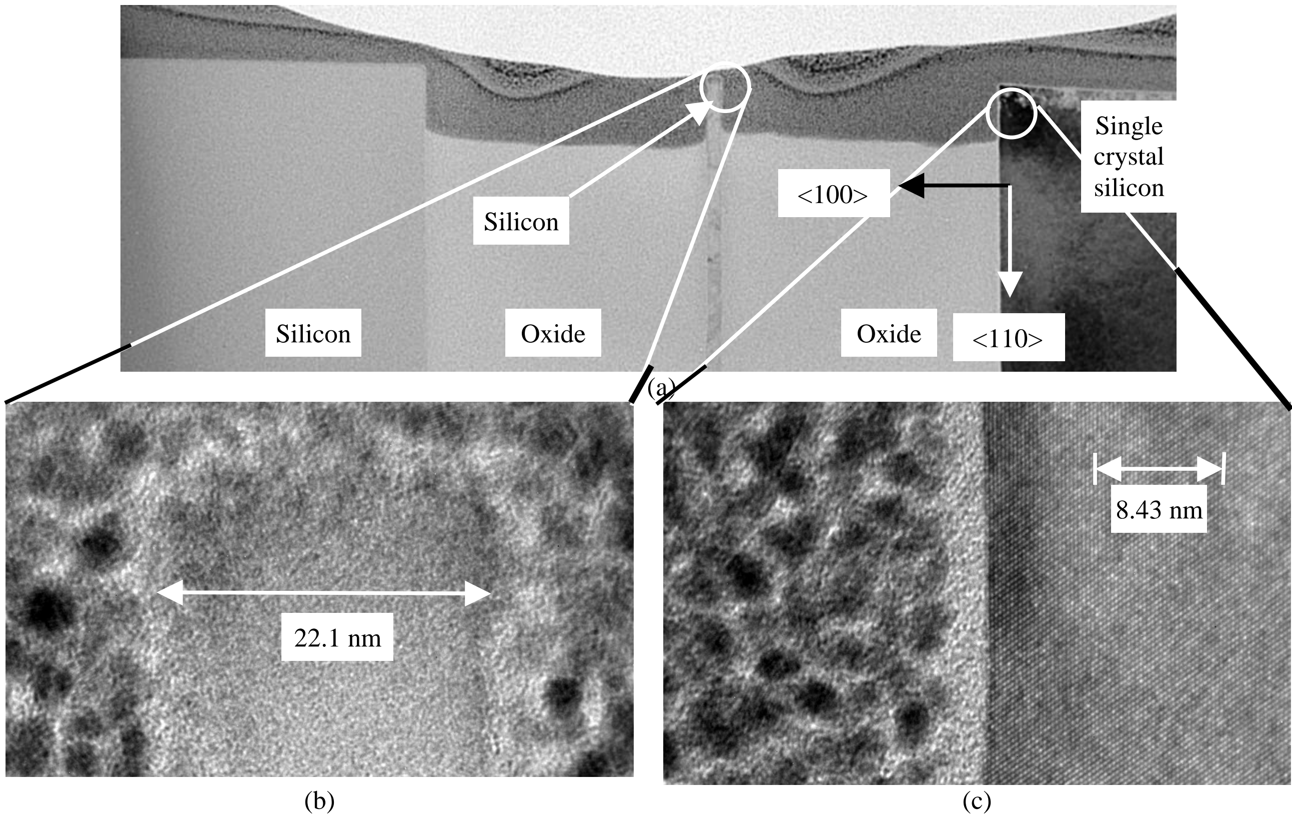

Fig. 9: TEM images of a line sample. These images were used to measure the width of the sample against the scale provided by the silicon atomic lattice spacing.

To prepare the sample for TEM, a section of the sample was first coated with platinum in a dual beam FIB/SEM system, then cut with the FIB and plucked. The sample was thinned in an ion mill and laid on a carbon film for TEM imaging. Because of the different sample preparation, the quality of the TEM image is not as good as the quality of the image shown for the trench sample. In principle, however, nothing would have prevented us from preparing the sample by

mechanical polishing. We chose the plucking technique because we wanted to save the sample for further studies. Fig. 9a shows a low resolution TEM cross section of the sample. The silicon line is seen protruding out of the deposited oxide in the middle of the sample. The silicon line is not made from single crystal silicon. Therefore we recorded a HRTEM image of the single crystal silicon from the silicon wafer to the right of the line showing the silicon atomic lattice (Fig. 9c). Then, without changing any imaging parameters, we moved the line under the electron beam and recorded a HRTEM image of the line (Fig. 9b). We then used the scale provided by the silicon atomic lattice spacing to the right of the line as a scale for the image of the line. This technique will inevitably add components of uncertainty to the technique illustrated for the trench. For example, because the sample is warped due to how thin it is, a cosine angle error must be taken into account. Using this procedure we measured the line width to be 22.1 nm. Like in the case of the trench measurement described above, this does not in itself constitute a traceable measurement because it is not accompanied with a statement of uncertainty. Nevertheless this example shows the traceability path that could be used to obtain a traceable measurement of the line structure.

4. STRUCTURES WITH NON-VERTICAL SIDEWALLS

A slight variation of the technique can be used to fabricate samples with a predetermined sidewall angle. For example, to build a trench with a non-vertical sidewall angle one could proceed as described above for the case of the trench sample. However, the final polishing step would be done with the sample tilted with respect to the polishing wheel to obtain the structure shown in Fig. 10. When top reference mounted, the polished surface will be coplanar with the surface of the wafer and the polishing angle rotates into a sidewall angle.

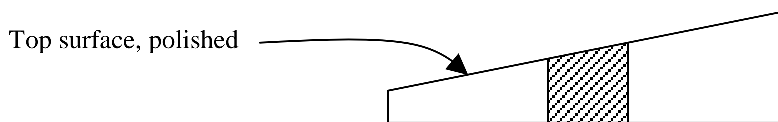

Fig. 10: The surface of the sample can be polished at an angle with respect to the direction of the trench to create two supplementary sidewall angles between the trench and the surface of the sample.

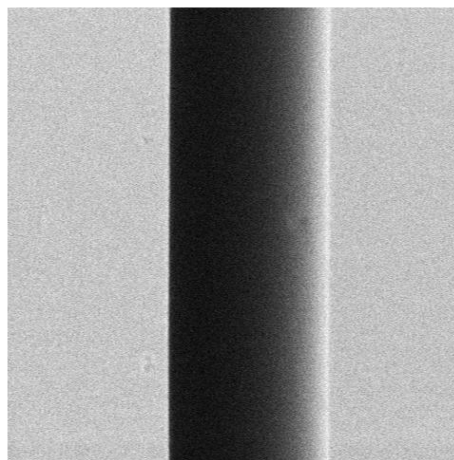

Fig. 11: CD-SEM image of a 500 nm trench with built-in sidewall angles of nominal 95 degrees (left) and nominal 85 degrees (right).

The sidewall angle can be measured and certified by looking at the sample from its side with a low magnification optical microscope, as the trench, which extends through the entire thickness of the sample, scatters enough light to be visible. This technique provides on the same samples two sidewall that are rigorously supplementary. Fig. 11 shows a CD-SEM image of a 500 nm wide trench polished at an angle of 5 degrees. The trench was etched to a depth of several microns. We chose a wide trench for this application to minimize proximity effects between the two edges. Notice that

the reentrant angle provides a knife-edge structure and may be ideally suited for a variety of CD-SEM and AFM characterization purposes.

5. APPLICATIONS

We envision a number of possible applications for the types of structures described in this paper in the area of tool calibration, tool monitoring, tool matching, and process control of CD-SEM and CD-AFM tools. Although we have not developed those applications, we list here those that seem promising.

1. Absolute calibration of CD-SEM and CD-AFM metrology, traceable to the international system of units. The generally accepted current best practice methodology to measure bias and linearity of CD measurements is by using cross-section TEM or cross-section SEM measurements as reference[3]. Quality attributes of a reference samples are: 1) good uniformity of the reference feature along a reasonable length of line; 2) traceability to the silicon atomic lattice spacing or other accepted method; 3) feature size and material comparable to the size and materials of the features to be measured.
2. Determination of linearity of CD measurement tools. CD metrology in a CD-SEM is facilitated by the bright edges that form at topographic discontinuities in a surface. As feature sizes become smaller, the two bright edges start to interact with each other, and the algorithms used to determine the value of CD may have to be modified to guarantee measurement linearity. This task can be accomplished with the use of absolute standards of size comparable to the size of the features being measured.
3. Line edge roughness tool monitor. We propose the use of the trench sample as a zero line edge roughness monitor. The trenches that can be made with this technique are exceptionally smooth on a length scale of 1 μm or less. We are not aware of a sample that can be used in a CD-SEM, and which exhibits lower line edge roughness than this one. Therefore, it appears to be a good candidate for monitoring the noise level of line edge roughness measurement tools and algorithms. If a traceable value of line edge roughness had to be associated with the sample, it seems that it could be derived from cross-sectional TEM images.
4. Stray tilt calibration. Stray tilt can be a significant contributor to error in a CD-SEM measurement[4]. The stray tilt manifests itself as an asymmetric intensity profile from an otherwise symmetric feature. Because the line width samples presented in this paper have square corner and vertical sidewalls, they generate minimal widening in the intensity profile at the line edges, which facilitates the task of measuring the asymmetry in the intensity profile. It is important that any parasitic tilt in the sample to due errors in the angle of polishing, as well as any tilt due to the subsequent mounting into the pocket wafer be measured, certified, and taken into account in order to use the sample for stray tilt calibration.
5. Verification of model-based metrology algorithms. Model-based metrology for CD-SEM requires validation through a series of structures that simulate various material and topographical features of the structures, including feature height, width, slope, top corner radius, footing, and proximity effects[5]. The line samples presented in this paper offer the ability to arbitrarily vary the height, width, slope, and proximity effect, with some limitations with respect to the possible combinations of these effects. For example, in regards to slope, this technique does not allow the fabrication of a symmetric structure with sidewall angle other than 90 degrees.
6. Beam profile measurement. Taking advantage of the sharpness of the edges of the sample, whether mounted vertically or at a reentrant angle with respect to the electron beam of a CD-SEM, the sample can be used as a knife-edge to determine properties of the beam shape and to determine the ultimate resolution of the tool. The beam shape can be measured in a lateral direction by measuring the intensity profile as the beam scans across the knife-edge. It may also be possible to measure the beam profile in the vertical direction by measuring the intensity profile as the beam scans across the knife-edge when the sample is moved down from the best focus position. In addition, it is conceivable to use these samples in conjunction with a software simulation package to determine beam parameters such as numerical aperture and aberrations from a best fit between simulation of intensity profiles and actual line scan data. Fig. 12 shows a comparison between simulations and actual data for 12 nm, 25 nm, and 50 nm line width samples. The simulations[6] were done using a software package developed in house, which combines Monte-Carlo simulations inside the material with electron ray tracing outside the material, in a field that is calculated inside and outside the material using Laplace and Poisson's equations. The absorption of primary electrons within the material is used to account for charging effects.

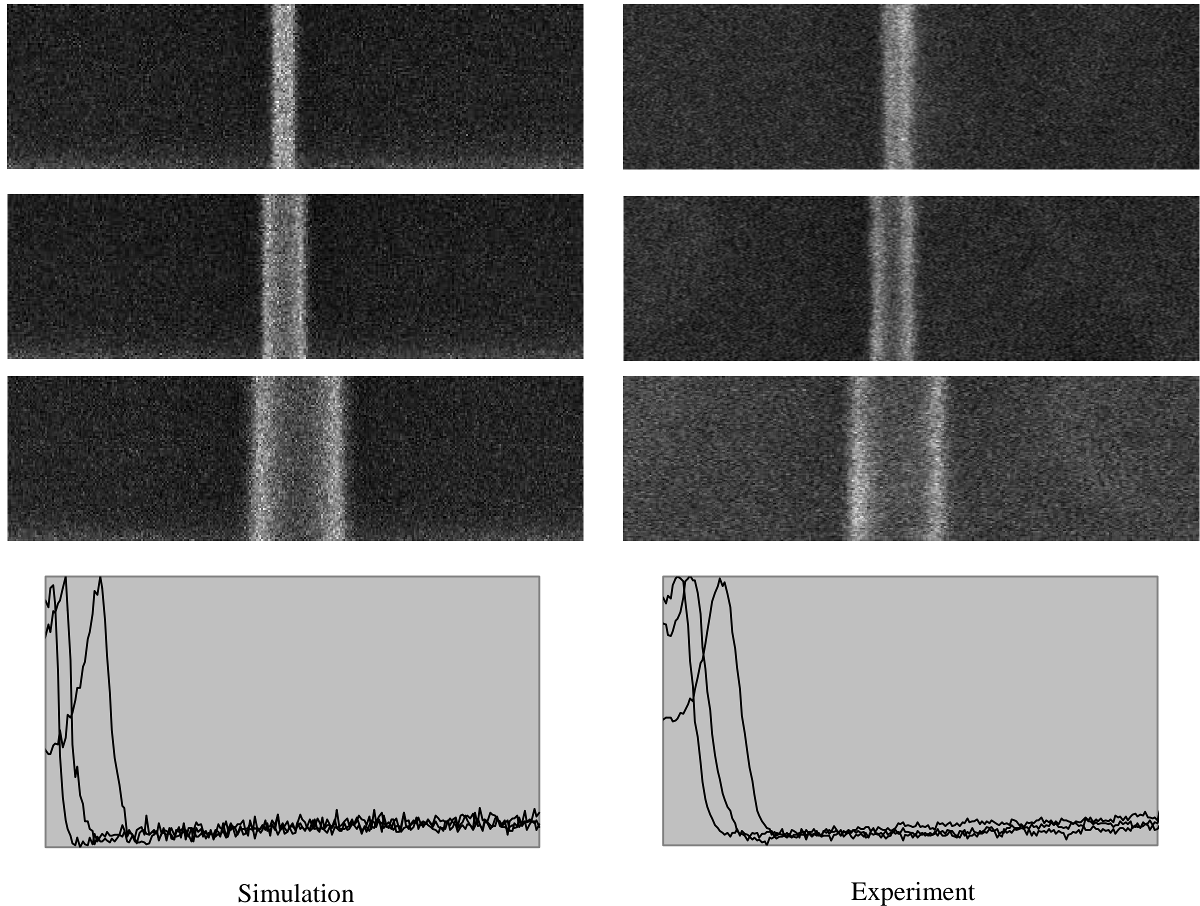

Fig. 12: Simulation and actual data of scan profiles across the 12 nm , 25 nm, and 50 nm line width samples.

6. CONCLUSIONS

We have presented a technology that takes advantage of the high uniformity of thin film deposition technologies to create lateral dimensional artifacts with uniformity properties typical of a deposition process. We have shown how to fabricate isolated silicon trench and isolated line width artifacts in the range of 12 nm to 500 nm, where the width, height, and slope can be varied. In the case of a line width the proximity effect due to a nearby silicon structure can be varied as well. The structures formed have top corner radii as small as 5 nm. It is possible to obtain a measurement of the critical dimensions of such structures from cross-section TEM images, although a rigorous measurement associated with an uncertainty has not been presented. These samples can be mounted into silicon wafers for use in automated CD-SEM and CD-AFM tools. We envision applications of these samples for the absolute calibration of CD measurements at various dimensions, thus enabling calibration of tool linearity, and for the assessment and monitoring of line edge roughness measurement capability. In addition, these samples may find use in CD-SEM metrology for stray tilt calibration, beam profile measurement, and for the verification of model-based metrology algorithms. Simulations of the intensity profiles show good agreement with the experimental results. While improvements in the area of line edge roughness of the line width samples and in the area of etch control are in order, we have not yet encountered a fundamental limit to the scaleability of the technology below 12 nm.

7. REFERENCES

1. M. W. Cresswell, E. H. Bogardus, J. V. Martinez de Pinillos, M. H. Bennett, R. A. Allen, W. F. Guthrie, C. E. Murabito, B. A. am Ende, and L. W. Linholm, "CD Reference Materials for Sub-Tenth Micrometer Applications", *Proc. SPIE* **4689**, 116-127 (2002).
2. M. Tortonese, J. Prochazka, P. Konicek, J. Schneir, and I. R. Smith, "100 nm Pitch Standard Characterization for Metrology Applications", *Proc. SPIE* **4689**, 558-564 (2002).
3. M. Sendelbach and C. Archie, "Scatterometry Measurement Precision and Accuracy below 70 nm", *Proc. SPIE* **5038**, 224-238 (2003).
4. E. Solecky, C. Archie, J. Mayer, R. Cornell, and O. Adan, "Characterizing and Understanding Stray Tilt: the Next Major Contributor to CD SEM Tool Matching", *Proc. SPIE* **5038**, 518-527 (2003).
5. J. S. Villarubia, A. E. Vladar, and M. T. Postek, "A Simulation Study of Repeatability and Bias in the CD-SEM", *Proc. SPIE* **5038**, 138-149 (2003).
6. L. Grella, G. Lorusso, D. L. Adler, "Simulations of Scanning Electron Microscopy Imaging and Charging of Insulating Structures", *Scanning* **25**, 300-308 (2003).